ELECTROMIGRATION PERFORMANCE OF WLCSP SOLDER JOINTS

Robert Darveaux Jimmy-Dinh V Hoang Bhuvaneshwaran Vijayakumar

Skyworks Solutions, Inc. 5221 California Ave. M/S 21-1 Irvine, CA 92617 robert.darveaux@skyworksinc.com

ABSTRACT

Wafer Level Chip Scale Package (WLCSP) assemblies were tested under high temperature and high current conditions. Electromigration damage was observed along with accelerated diffusion and intermetallic compound growth at the solder / Under Bump Metallization (UBM) interface. Final electrical failure typically occurred due to a void created in the redistribution line (RDL) near the UBM. The failure rate increased with higher temperature, higher current density, and reduced RDL trace width. Both Ni UBM pads and Cu pillar structures had superior performance over Cu UBM pads. A failure model based on Black's equation was developed from the experimental data and other published data. The model was then used to develop recommended guidelines for accelerated testing and qualification testing based on representative field use conditions.

Key words: WLCSP, electromigration.

INTRODUCTION

WLCSP has become a popular package for devices such as RF buck converters, camera flash drivers, backlight drivers, and analog switches used in portable product applications due to its small form factor. These devices require current of up to 2A or more to be delivered through BGA solder joints. One potential limiter to the maximum current rating for a given device is field failure due to electromigration.

Electromigration failure in flip chip and WLCSP solder joints occurs due to high current density driven diffusion and intermetallic compound reactions that are accelerated at high temperatures [1-34]. These effects can create voids that open up and grow over time. As the void size increases, there is an increase in electrical resistance through the joint, and eventually an open circuit occurs.

In most electromigration studies, design or material variables are compared using a test matrix of current densities and temperatures. The tests are often run until at least half of the units in a given leg have failed, so that the data can be fit to a log-normal or Weibull distribution. A typical goal is to determine constants for a failure prediction model, such as Black's equation [27].

In the present study, electromigration behavior of lead free WLCSP solder joints was studied with UBM diameters up to 300um, test currents up to 3.5A, and solder temperatures up to 194C. The sample size was 3 to 15 units per leg, and the test duration never exceeded 168hrs. Given this method and sample size, it was not always possible to get good Weibull statistics on every leg of the experimental matrix. However, several head-to-head evaluations were conducted, so the impact of multiple material and design variables could be quantified.

EXPERIMENTAL PROCEDURE

Three separate daisy chained test vehicles were used to study electromigration performance of lead free WLCSP solder joints. The bump lay out and daisy chain pattern for Test Vehicle (TV) #1 is shown in Figure 1a. For most of the experimental legs, eight bumps were used in the daisy chain. Only two bumps were used in one of the legs. TV#1 had three different UBM pad metal stack ups as indicated in Figures 1b, 1c, and 1d. The sputtered Ti/Cu layer between the UBM pad and RDL is not shown.

The bump pattern for TV#2 is shown in Figure 2a. Only a two bump chain was used in the testing. TV#2 had two different UBM pad stack ups. A 4-mask process stack up as shown in Figure 2b, and a 3-mask process stack up as shown in Figure 2c. The sputtered Ti/Cu layer between the UBM pad and RDL is not shown in Figure 2b.

The bump pattern for TV#3 is shown in Figure 3a. Only a two bump chain was used in the testing. The UBM pad stack up for TV#3 is shown in Figure 3b. This TV had both a single metal layer RDL configuration (as in Figure 3b), and a double metal layer RDL configuration.

In all cases, the motherboard had copper defined pads that were finished with organic surface protectant (OSP). The WLCSPs were surface mounted using a conventional reflow profile and a flux dip process.

Electromigration testing was conducted under constant current and constant oven ambient temperature conditions. In all cases, the test duration was 168hrs.

a. Bump layout.

b. Stack up 1. Dimensions in (um).

c. Stack up 2. Dimensions in (um).

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b. Stack up 1. Dimensions in (um).

c. Stack up 2. Dimensions in (um). **Figure 2.** Test vehicle #2. Two bump chain used.

Shown in Figure 4 is the original printed circuit board (PCB) configuration used in Legs 1 to 18. Nine units were surface mounted to the PCB, and thermocouples were soldered near each component to monitor the local temperature. It was found that joule heating in the PCB caused non-uniform test temperatures for the WLCSPs. Hence the test data was divided into three groups as indicated in Figure 5. Therefore, the effective sample size was three units for legs 1a through 11c.

To improve the temperature uniformity, individual PCBs were applied for each WLCSP as shown in Figure 6. The sample size was increased to fifteen units per leg for data sets 13 to 83. Thermocouples were soldered to each test board to monitor the local temperature. A summary of the experimental variables is shown in Table 1.

a. Bump layout.

b. Stack up.

Figure 3. Test vehicle #3. Two bump chain used.

Figure 4. Nine-unit evaluation board inside oven for data sets 1 through 11.

Figure 5. Three groups of units based on temperature distribution from joule heating in evaluation board.

Figure 6. Fifteen individual evaluation boards in oven for data sets 13 through 83.

| UBM Pad Stack Up (um) | 0.65 Ni / 0.70 Cu, 2 Ni, | |
|---------------------------|--------------------------------|--|
| | 7.5Cu/2.5Ni, 10Cu, 50Cu | |
| UBM Diameter (um) | 160 to 300 | |
| PCB Pad Diameter (um) | 220 to 250 | |
| Solder Ball Diameter (um) | 167 to 300 | |
| RDL Width (um) | 90 to 340 | |
| Solder Alloy | SAC305, SAC405 | |
| Joints in Daisy Chain | 2 to 8 | |
| Current (A) | 1.8 to 3.5 | |
| Oven Temperature [C] | 85 to 154 | |
| PCB Temperature [C] | 103 to 164 | |
| Solder Temperature [C] | 129 to 194 | |
| Test Duration (hrs) | 168 | |

Table 1. Range of Experimental Variables

ESTIMATION OF SOLDER JOINT TEMPERATURE

Finite element analysis was used to estimate the solder temperature during electromigration testing for each leg in the experiment. The power dissipation from joule heating in the daisy chain traces was calculated from the measured resistance and the applied current. The power was allocated over the different portions of the daisy chain depending on the PCB and RDL trace cross section. The oven ambient temperature was a boundary condition in the model, and the temperature distribution was solved using $ANSYS^{TM}$. The convective heat transfer coefficients were adjusted until the calculated PCB temperature matched the measured value.

Example calculated temperature distributions are shown in Figures 7, 8, and 9 for TV#1, TV#2, and TV#3, respectively. It is seen that the 8-bump daisy chain case in Figure 7 results in much more uniform die temperature compared to the 2-bump daisy chain cases in Figures 8 and 9. Also, the temperature rise due to joule heating is much greater in Figures 7 and 9 compared to Figure 8 due to the higher DC resistance of the daisy chains.

Figure 7. Example calculated temperature distribution for TV #1, Leg 2a, 8-bump daisy chain. **Board temp = 137C (Solder ball temp = 158C)**

Figure 8. Example calculated temperature distribution for TV#2, Leg 73a, 2-bump daisy chain. **Board temp = 156C (Solder ball temp = 160C)**

Board temp = 136C (Solder ball temp = 155C)

Figure 9. Example calculated temperature distribution for TV #3, Leg 81, 2-bump daisy chain.

EXPERIMENTAL RESULTS

A summary of all test results is shown in Table 2. There were a total of thirty three data sets with a sample size of three units, and sixteen data sets with a sample size of fifteen units. The key design attributes are shown in Table 2, as well as the test conditions and results after 168hrs of testing.

Failure Mechanism

The failure mechanism was similar for all test vehicles and experimental conditions evaluated in the present study. Electromigration damage was observed due to accelerated diffusion and intermetallic compound growth at the solder / UBM interface. Final electrical failure typically occurred due to a void created in the RDL near the UBM. A representative cross section of a failed unit is shown in Figure 10. A similar failure mode in WLCSP solder joints was observed in Refs [22,28,34]

A representative resistance log for a nine sample population is shown in Figure 11. There is a steady increase in resistance for all units on test due to conversion of the copper and solder into intermetallic compounds. However, a rapid increase in resistance is detected when a void starts to develop in the UBM and RDL regions as indicated by samples C4, C5, and C6 in Figure 11.

Effect of Solder Temperature

Electromigration performance degraded with an increase in solder temperature. This effect was demonstrated by reducing the RDL width or increasing the oven temperature.

The temperature effect is seen by comparing legs 3a-c with legs 1a-c. The RDL width was 90um in legs 3a-c and 270um wide in legs 1a-c. This resulted in more joule heating, a 37C to 50C higher solder temperature, and a much higher failure rate for legs 3a-c.

The temperature effect is also seen in comparing the superior performance of legs 4a-c and 5a-c over legs 3a-c. Reduced oven temperatures resulted in 28C to 51C lower solder temperatures, and better electromigration performance.

Effect of Current Density

Electromigration performance degraded with an increase in current density. This effect was demonstrated by increasing the test current, or by decreasing the UBM diameter.

The electromigration performance degradation due to increasing test current is seen in the following combinations: leg 2b versus 1b, leg 17 versus 15, and legs 81,82 versus 80,83.

The electromigration performance degradation with a decrease in UBM diameter is seen in the following combinations: leg 3b versus 3c, and legs 6a-c versus 7a-c.

The effect of decreasing UBM diameter was also observed in Refs [30,31,33].

Effect of RDL Width

Electromigration performance is degraded with a decrease in RDL width for three reasons: 1) the current crowding effect increases the local current density, 2) the joule heating increases, and 3) a smaller void is required to cause a resistance increase in eventual open circuit. The negative impact of decreased RDL width is seen by comparing legs 3a-c versus 1a-c. Similar observations of increased current crowding, increased joule heating and reduced lifetime due to decreased RDL width were made in Refs [25,30,31].

Effect of UBM Pad Stack

Several UBM pad stacks were evaluated using across the three test vehicles. For samples with a 240um to 250um UBM diameter, a tall copper pillar (50um height) and a 2um Ni UBM performed the best.

The copper pillar structure has at least three advantages: 1) reduced current crowding to minimize localized high current density, 2) reduced joule heating, and 3) provides a distance barrier so solder cannot directly react with the copper RDL. The improved performance of copper pillar samples can be seen in the following combinations: legs 10a-c versus 3a-c, and leg 13 versus 17. Excellent electromigration performance of copper pillar structures was also observed in Refs [14,15,23].

The 2um Ni UBM improves electromigration performance by providing a metallurgical barrier that prevents reaction of the solder and copper RDL. This effect can be seen by comparing legs 73a-c versus legs 17 and 18. A similar trend was reported in Ref [34].

It should be noted that a 2.5um Ni layer on top of a 7.5um Cu pad does not act as an effective metallurgical barrier. The solder is able to wet to the copper pad edge and provide a path where the copper RDL can react with Sn. The failure shown in Figure 10 is such an example. Also, it is seen that legs 6a-c and 7a-c with the Cu/Ni pad had similar or worse performance than legs 8a-c and 9a-c with a Cu pad.

However, the 0.65umNi/0.70umCu pad used in TV#3 does provide a reasonable metallurgical barrier to protect the Cu RDL trace. The performance of legs 80 to 83 with a 160um UBM diameter was comparable to legs 15 to 18 with a 250um UBM diameter.

DISCUSSION

Electromigration failure data is commonly fit to some form of Black's equation [27]

$$
t = AJ-n exp(Ea/kT)
$$
 (1)

where t is the time to failure, J is the current density, T is temperature, and k is Boltzman's constant. The constants

A (pre-factor), n (current density exponent), and E_a (activation energy) are constants applicable to a given metallurgical system. In a typical evaluation, a matrix of test temperatures and current densities is defined and the constants A, n, and E_a can be determined.

The current study is not conducive to easily determining the Black's equation constants because 1) many of the tests were not extended until 50% of the population had failed, 2) legs 1 through 11 had only three unit sample sizes, and 3) multiple test parameters (current, temperature, RDL width) were varied at once. Nevertheless, it is possible to compare the present results with those in literature by making some reasonable assumptions.

Figure 10. Cross section of failed solder joint. Leg 6a, TV#1, 7.5um Cu / 2.5um Ni UBM pad, 250um UBM diameter, 90um RDL trace width, 1.8A, 177C, 69hrs.

Figure 11. Resistance increase during electromigration failure for 3of 9 units. Leg 7, TV#1, 7.5um Cu / 2.5um Ni UBM pad, 300um UBM diameter, 90um RDL trace width, 1.8A, 178C to 190C solder temperature.

Table 2. Summary of test results.

Previous studies on lead free flip chip and WLCSP assemblies were used to select constants for Black's equation. The range of current density exponent, n, in Refs [3,7,8,9,13,16,19,29,33] was 1.0 to 9.8. We used a value of 2.0 in the present analysis. The current density was calculated using the UBM pad area. The range of measured activation energy, E_a , in Refs $[3,7,9,13,16,19,20,22,29,32]$ was 0.5 to 1.6eV. We used a value of 1.0eV in the present analysis. Based on these constants, the data of Gee et.al. [20] were used to estimate the pre-factor, A in Eq.(1). The median failure (t50%) of each test condition in Ref [20] was used to estimate A as $2.2E-6$ hrs/ $(A/mm^2)^{2.0}$.

Sixteen data sets in Table 2 had at least 1 measured failure. Seven of the data sets had enough failures to determine t50% directly. The average Weibull shape parameter (slope) was 2.57 for these data sets. The remaining nine data sets did not have enough failures to determine t50% directly, so the average Weibull shape parameter of 2.57 was applied to estimate t50%.

Shown in Figure 12 is a plot of calculated versus measured electromigration life using the Black's equation constants discussed above. It is seen that the data from Ref [20] were well fit to the model. However, the model correlation for the present study's data depends on the UBM metal stack. The 7.5um Cu / 2.5um Ni and 10um Cu data are above the line, and hence they perform slightly worse than the data from Ref [20]. The 0.65um Ni / 0.70um Cu data are below the line, so this data set performs better than that from Ref [20]. This is likely due to the fact that Gee et.al. UBM stack had a thinner Ni layer (0.32um Ni / 0.8um Cu) [20].

It was assumed that only the pre-factor, A, varies with UBM metal stack. Hence, a simple ratio of calculated to measured life was used to estimate the pre-factor for each case. A summary of the proposed Black's equation constants for the various UBM metal stacks is shown in Table 3.

The 2um Ni and 50um Cu UBM metal stacks did not fail under the test conditions studied here. In order to estimate the worst case pre-factor, A, it was assumed that a failure could have occurred at 169hrs of the most aggressive test condition evaluated. Then, the t50% life was estimated using a Weibull shape factor of 2.57.

Shown in Figure 13 is a plot comparing the worst case t50% performance for 2um Ni and 50um Cu UBM metal stacks versus the calculated life using Gee et.al. Black's constants. The data points are below the line, which indicates better performance than the baseline case from Ref [20]. The minimum estimated pre-factor, A, was calculated for 2um Ni and 50um Cu UBM pad stacks as shown in Table 3. It is likely that these pre-factors are conservative, since no actual failures were recorded.

Electromigration testing is not a well-established method with respect to typical device qualification. A proposed accelerated test and qualification test based on an example field use reliability criteria for consumer product applications is given in Table 4. If one assumes that the field use environment has a PCB temperature of 60C and there is 21C of joule heating, then the solder temperature is 81C. The specified acceptable cumulative failures are < 0.1% after 1yr (8760hrs) of service.

For the qualification test, the sample size is 77 units, so the first failure would constitute a median rank cumulative distribution of 0.9%. The test duration is 1000hrs at rated current. If the joule heating is 25C, then the PCB should be maintained at 92C to achieve a solder temperature of 117C. Passing such a qualification test should be equivalent to passing the stated field use condition.

Figure 12. Correlation of calculated versus measured electromigration performance.

Figure 13. Estimated minimum performance of 2um Ni UBM and Copper Pillar WLCSPs that had no failures in the present evaluation.

For the accelerated test, the sample size is 15 units, so the first failure would constitute a median rank cumulative distribution of 4.5%. The test duration is 168hrs at rated current. If 25C of joule heating is assumed, then the PCB should be maintained at 127C to maintain a solder temperature of 152C. Passing such an accelerated test should be equivalent to passing the qualification conditions or the field use conditions.

| UBM Metal Stack | | n | E, |
|------------------------|------------------------|-----|---------|
| | $(hrs/(A/mm^2)^{2.0})$ | | e v |
| Gee. et.al. [20] | $2.2E-6$ | 2.0 | 1.0 |
| 7.5um Cu / 2.5um Ni | $1.1E-6$ | 2.0 | 1.0 |
| 10um Cu | 1.8E-6 | 2.0 | 1.0 |
| 0.65um Ni / 0.70um Cu | $7.0e-6$ | 2.0 | 1.0 |
| 2um Ni | $> 1.0e-5$ | 2.0 | $1.0\,$ |
| 50um Cu | $> 5.5e-6$ | 2.0 | 10 |

Table 3. Recommended Black's equation constants assuming only pre-factor, A, varies with the UBM metal stack.

Table 4. Proposed accelerated test and qualification test conditions based on example field use reliability requirement and environment. Assumed that $E_a = 1.0$ eV, Weibull shape parameter (slope) $= 2.57$, and device is tested at rated max current level.

CONCLUSIONS

1) Electromigration failure of WLCSP assemblies was found to occur due to a void created in the RDL trace near the UBM pad.

2) The failure rate increased with higher temperature, higher current density, and reduced RDL trace width.

3) A Ni UBM pad and a Cu pillar structure had the best performance of the metal stacks tested.

4) A failure model based on Black's equation was developed from both the experimental data and other published data. The model was then used to develop recommended guidelines for accelerated testing and qualification testing based on representative field use conditions.

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